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C. Amendments to the Claims.

1. (Original) A semiconductor device including an insulated gate field effect transistor (IGFET), comprising:

5 a gate electrode of the IGFET having a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode;

a cap film formed on the upper layer electrode;

a first nitride film on a side surface of the upper layer electrode;

10 an oxide film on a side surface of the lower layer electrode; and

an etching stopper film including a second nitride film formed on the outside of the first nitride film and oxide film.

2. (Original) The semiconductor device according to claim 1, wherein:

first nitride film is a thermal nitride film.

15 3. (Original) The semiconductor device of claim 2, wherein:

first nitride film is a rapidly heated thermal nitride film.

4. (Original) The semiconductor device of claim 2, wherein:

the first nitride film has a film thickness of approximately 2 to 5 nm.

20 5. (Original) The semiconductor device of claim 2, further including:

an interlayer insulating film formed to cover the gate electrode of the IGFET;

a contact hole opened in the interlayer insulating film to expose a source/drain region of the IGFET; and

25 a conductor filling the contact hole and electrically connected with the source/drain region.

6. (Original): The semiconductor device of claim 2, wherein:

the oxide film is a thermal oxide film.

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7. (Original): The semiconductor device of claim 2, wherein:

the second nitride film is formed with chemical vapor deposition (CVD).

8. (Cancelled) A method for manufacturing a semiconductor device including an insulated gate field effect transistor (IGFET), comprising the steps of:

5 forming a gate insulating film on a semiconductor substrate;

forming a laminate film on the gate insulating film, the laminate film including an insulating film formed on a second conductive film formed on a first conductive film;

10 etching the insulating film and second conductive film into a predetermined pattern to form a cap layer and an upper layer gate electrode;

forming a first nitride film, that is a thermal nitride film, on the side surface of the upper layer gate electrode;

etching the first conductive film using the cap layer, upper layer gate electrode, and the nitride film as a mask to form a lower layer gate electrode;

15 forming a first oxide film on the side surface of the lower layer electrode;
and

forming an etching stopper film including a second nitride film over the entire surface.

9. (Cancelled) The method for manufacturing a semiconductor device of claim 8, wherein:

20 the first conductive film includes a polysilicon film; and

the second conductive film includes a metal film.

10. (Cancelled) The method for manufacturing a semiconductor device of claim 8, wherein:

the first conductive film includes a polysilicon film; and

the second conductive film includes a metal silicide film having a high
25 melting point.

11. (Cancelled): The method for manufacturing a semiconductor device of claim 8, wherein

the first oxide film is a thermal oxide film.

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12. (Cancelled) The method for manufacturing a semiconductor device of claim 8, wherein:
5 forming the etching stopper film includes forming the second nitride film with a chemical vapor deposition.

13. (Cancelled) The method for manufacturing a semiconductor device of claim 8, wherein:
5 the first nitride film is a thermal nitride film formed with a rapid thermal nitridation step using a lamp as a heat source.

14. (Cancelled): The method for manufacturing a semiconductor device of claim 8, further including the steps of:

10 forming a source/drain region by doping an impurity into the semiconductor substrate after the step of forming the first oxide film; and

forming an interlayer insulating film over the entire surface and selectively etching the interlayer insulating film with a selective etching ratio for the etching stopper film to open a contact hole after the step of forming the etching stopper film.

15 15. (Cancelled) The method for manufacturing a semiconductor device of claim 8, further including the steps of:

forming a LDD (lightly doped drain) region by doping a first impurity concentration into the semiconductor substrate after the step of forming the first oxide film;

20 anisotropic etching the etching stopper film to form a side wall etching stopper film on side surfaces of the lower layer gate electrode, upper layer gate electrode and cap layer; and

25 forming a source/drain region by doping a second impurity concentration into the semiconductor substrate using the side wall etching stopper film as a mask wherein the first impurity concentration is lower than the second impurity concentration.

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16. (Cancelled): The method for manufacturing a semiconductor device of claim 15, further including the steps of:

- forming a second oxide film over the entire surface of the substrate with a chemical vapor deposition method;
- 5 anisotropic etching the second oxide film to form a side oxide film on the side surface of the etching stopper film; and
- forming the source/drain region after the step of forming the side wall.

17. (Currently Amended) A semiconductor device including a first region and a second region, comprising:

- 10 a first gate electrode of a first IGFET in the first region having a first lower layer electrode formed on a first gate insulating film and a first upper layer electrode formed on the first lower layer electrode;
- a first cap film formed on the first upper layer electrode;
- a first nitride film on a side surface of the first upper layer electrode;
- 15 a first oxide film on a side surface of the first lower layer electrode;
- a first etching stopper film including a second nitride film formed on the outside of the first nitride film and first oxide film;
- a second gate electrode of a second IGFET in the second region having a second lower layer electrode formed on a second gate insulating film and a second upper layer electrode formed on the second lower layer electrode;
- 20 a second cap film formed on the second upper layer electrode;
- a third nitride film on a side surface of the second upper layer electrode;
- a second oxide film on a side surface of the second lower layer electrode;
- 25 a second etching stopper film including a fourth nitride film formed on the outside of the third nitride film and second oxide film; and
- wherein the first IGFET includes a lightly doped drain and the second IGFET does not include a lightly doped drain.

18. (Original) The semiconductor device of claim 17, wherein:

- the semiconductor device is a semiconductor memory device.

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19. (Original) The semiconductor device of claim 18, wherein:

the first region is a memory cell region and the second region is a peripheral circuit region.

20. (Original) The semiconductor device of claim 19, further including:

5 a first contact providing an electrical connection to a first source/drain region of the first IGFET;

a second contact providing an electrical connection to a second source/drain region of the second IGFET; and

10 a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode.

21. (New) A semiconductor device, comprising:

a first transistor formed in a first region comprising

15 a first upper layer gate electrode formed on and in electrical connection with a corresponding first lower layer gate electrode,

a first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode,

20 a second insulating film formed on a side surface of the first upper layer gate electrode, the second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and

25 a first etching stopper film formed on the outside of the first and second insulating films.

22. (New) The semiconductor device of claim 21, wherein:

the second insulating film comprises a thermal nitride film having a thickness of less than 6 nm.

30 23. (New) The semiconductor device of claim 21, wherein:

the first insulating film comprises a thermal silicon dioxide film.

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25. (New) The semiconductor device of claim 21, wherein:

the etching stopper film comprises a chemical vapor deposition silicon nitride film.

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26. (New) The semiconductor device of claim 21, wherein:

the first lower layer gate electrode has a greater gate length than the first upper layer gate electrode.

10 27. (New) The semiconductor device of claim 21, further including:

a second transistor formed in a second region comprising

a second upper layer gate electrode formed on and in electrical connection with a corresponding second lower layer gate electrode,

a third insulating film formed on a side surface of the second lower layer gate electrode and not on the side surface of the second upper layer gate electrode,

a fourth insulating film formed on a side surface of the second upper layer gate electrode, the fourth insulating film having a lower thermal growth rate with respect to the second upper layer gate electrode material than the thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material,

a second etching stopper film formed on the outside of the third and fourth insulating films,

a first transistor source/drain region extending laterally below the second etching stopper film, and

25 a second transistor source/drain region overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film.

28. (New) The semiconductor device of claim 27, further including:

30 a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film.

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29. (New) The semiconductor device of claim 28, further including:

the first transistor includes at least a third transistor source/drain region;

a first contact in electrical connection with the third source/drain region,

5 and isolated from the first lower layer gate electrode by a first insulating thickness; and

a second contact in electrical connection with the first and second source/drain regions, and isolated from the second lower layer gate electrode by a second insulating thickness that is greater than the first insulating thickness.